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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,203	10/29/2003	Jeffrey F. Hanson	03-1433	7329

24319 7590 01/10/2006

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,203	HANSON ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-11 and 15-18* is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/29/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to applicants' Amendment and Remarks filed on 10/27/2005 regarding application 10/696,203 filed on 10/29/2003. Claims 12 – 14, 19 and 20 have been cancelled. Claims 1 – 11 and 15 – 18 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 2, before "steps" delete —**the**—.
Claim 1, line 5, before "defects" insert —**physical**—.
Claim 1, line 6, before "defects" insert —**physical**—.
Claim 2, line 1, before "defects" insert —**physical**—.
Claim 3, line 1, before "defects" insert —**physical**—.
Claim 6, line 1, change "the step" to —**a step**—.
Claim 6, line 2, before "defects" insert —**physical**—.
Claim 7, line 1, change "the step" to —**a step**—.
Claim 8, line 1, change "the step" to —**a step**—.
Claim 9, line 2, before "steps" delete —**the**—.
Claim 9, line 7, before "structure" insert —**physical**—.
Claim 9, line 12 (2 places), before "defects" insert —**physical**—.
Claim 9, line 13, before "defects" insert —**physical**—.
Claim 9, line 14, before "defects" insert —**physical**—.
Claim 9, line 15, before "defects" insert —**physical**—.
Claim 9, line 16, before "defect location" insert —**physical**—.
Claim 9, line 19, before "defects" insert —**physical**—.
Claim 10, line 1, before "defects" insert —**physical**—.
Claim 10, line 2, before "defect wafer" insert —**physical**—.
Claim 11, line 1, before "defects" insert —**physical**—.
Claim 11, line 2, before "defects" insert —**physical**—.
Claim 15, line 1, change "the step" to —**a step**—.
Claim 16, line 1, before "defects" insert —**physical**—.
Claim 16, line 1, change "the system" to —**the computerized system**—.

Claim 16, line 7, before "structures" insert —**physical**—.
Claim 16, line 7, change "the database" to —**a database**—.
Claim 16, line 11, before "defect information" insert —**physical**—.
Claim 16, line 11, before "defects" insert —**physical**—.
Claim 16, line 12, before "defect information" insert —**physical**—.
Claim 16, line 13, before "defects" insert —**physical**—.
Claim 16, line 15, before "defects" insert —**physical**—.
Claim 17, line 1, change "The system" to —**The computerized system**—.
Claim 17, line 1, before "defects" insert —**physical**—.
Claim 17, line 2, before "defect wafer" insert —**physical**—.
Claim 18, line 1, change "The system" to —**The computerized system**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,707,936 B1 to *Winter et al.* in view of U.S. Patent No. 5,475,695 to *Caywood et al.*

5. As to Claim 1, *Winter et al.* show and disclose the following subject matter:

- *Manufacturing (physical) defect* will cause an electrical failure in an actual device fabricated according *design information* – [abstract]; *actual (physical) defects* are *visually inspected* by microscope – [col. 4, line 2 – 9]; inspected features are stored in a database 28 – [Fig. 3];
- A *wafer* (i.e., *substrate*) includes *a plurality of semiconductor devices* which are each fabricated according to (respective) *device design information* – [Fig. 1; col. 2, line 28 – 37]; Notice that (1) the plurality of semiconductor devices could belong to *different classes* and have different device design information, which are stored in a database for retrieval;
- Inspecting a part (i.e., wafer) fabricated according *design information* to *identify defects* therein and at least one characteristic of each (physical) defect – [col. 1, line 58 – 64]; Each defect has associated characteristics, such as a size of the defect...a *location* of the defect – [col. 2, line 49 – 56]; Notice (1) locations of physical defects are stored in the database 28 (2) that the inspecting is performed by comparing the database of physical defects on the wafer (substrate) to a database of design information of semiconductor devices.

Winter et al. do not disclose a step of associating physical defects on the wafer with classes of design information by location on the wafer of both the physical defects and elements of the design information to produce yield enhancement data. But *Caywood et al.* teach this step – [col. 1, line 29 – 37]. *Caywood et al.* teach this the following subject matter:

- Using design information to identify electrical node-to-node faults caused by fabrication (physical) defect – [abstract];
- Location of fabrication (physical) defect that caused electrical fault must be identified – [col. 1, line 29 – 31];
- Identifying (locations of physical) defects which are most important in limiting yield and then to take appropriate action to reduce the occurrence of those (physical) defects thereby generating yield enhancement data for achieving yield improvement – [col. 1, line 34 – 37].

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of *Caywood et al.* in associating physical defects on a wafer with classes of design information by location on the wafer of both the physical defects and elements of the design information in order to identify which defects are most important in limiting yield thereby producing yield enhancement data for use in reducing the occurrence of those physical defects.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

6. As to Claim 2, *Winter et al.* show a defect wafer map in Fig. 1.

7. As to Claim 3, reasons are included in **[Response A]** given above. *Winter et al.* disclose using microscope to visually inspect actual (physical) defects – [col. 4, line 2 – 9].

8. As to Claims 4 and 5, reasons are included in **[Response A]** given above. *Caywood et al.* disclose using design information in identifying node-to-node faults of IC products – [abstract]. Therefore, the design information includes node-to-node structures formed in semiconductor devices in the wafer. Classes of design information comprise classes of physical structures.

9. As to Claim 6, *Winter et al.* disclose the subject matter (multiple past inspections of various different wafer) – [col. 3, line 62 – 65].

10. As to Claim 7, it is well known in the art that design information of each integrated circuit device is stored in a separate design file. All design filed are stored in a design database for future retrieval.

11. As to Claim 8, reasons are included in **[Response A]** given above. *Caywood et al.* disclose using *correct action* (i.e., *appropriate action*, *revising design information*) to reduce occurrence of defects which limits yield thereby achieving yield improvement – [col. 1, line 34 – 37; line 49]

Allowable Subject Matter

12. Claims 9 – 11 and 15 – 18 are allowed. Those claims are allowed is because the prior art does not teach or suggest the following subject matter:

- A method for producing yield enhancement data from integrated circuits on a substrate, the method comprising a step of *binning physical structures in design information in a database of design information as belonging to at least one of a number of different classes of physical structures* in combination with other limitations as recited independent **Claim 9**;
- A computerized system for analyzing physical defects, the computerized system comprising *means of binning physical structures in design information in a database of design information as belonging to at least one of a number of different classes of physical structures* in combination with other limitations as recited independent **Claim 16**.

Response to Amendment and Remarks

13. Applicants' amendments and remarks filed on 10/27/2005 have been reviewed. Applicants' arguments, based on amended limitations, have been fully considered. Responses are revised based on newly found prior art. Detailed responses are given above.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sun James Lin
Patent Examiner
Art Unit 2825
January 5, 2006